OIPE JC16
MAY 12 2004
PATENT & TRADEMARK OFFICE

FIG. 1
(BACKGROUND ART)

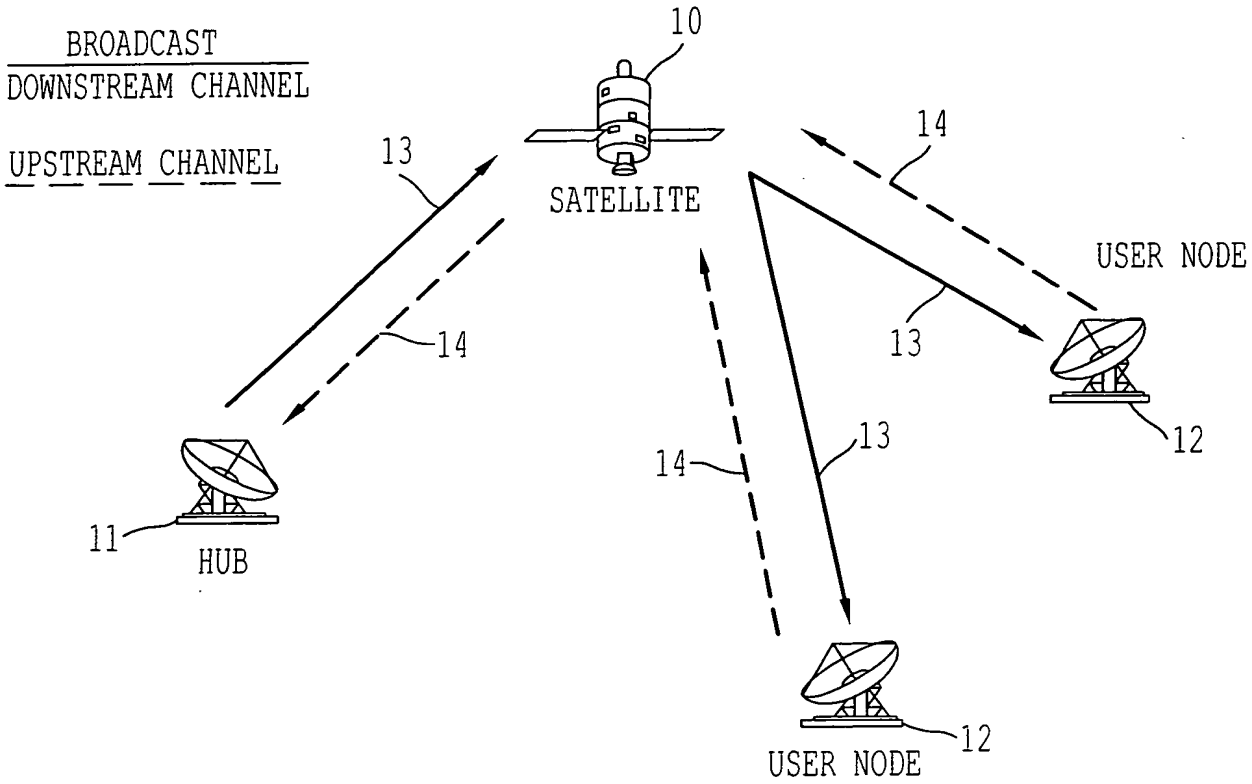


FIG. 2
(BACKGROUND ART)

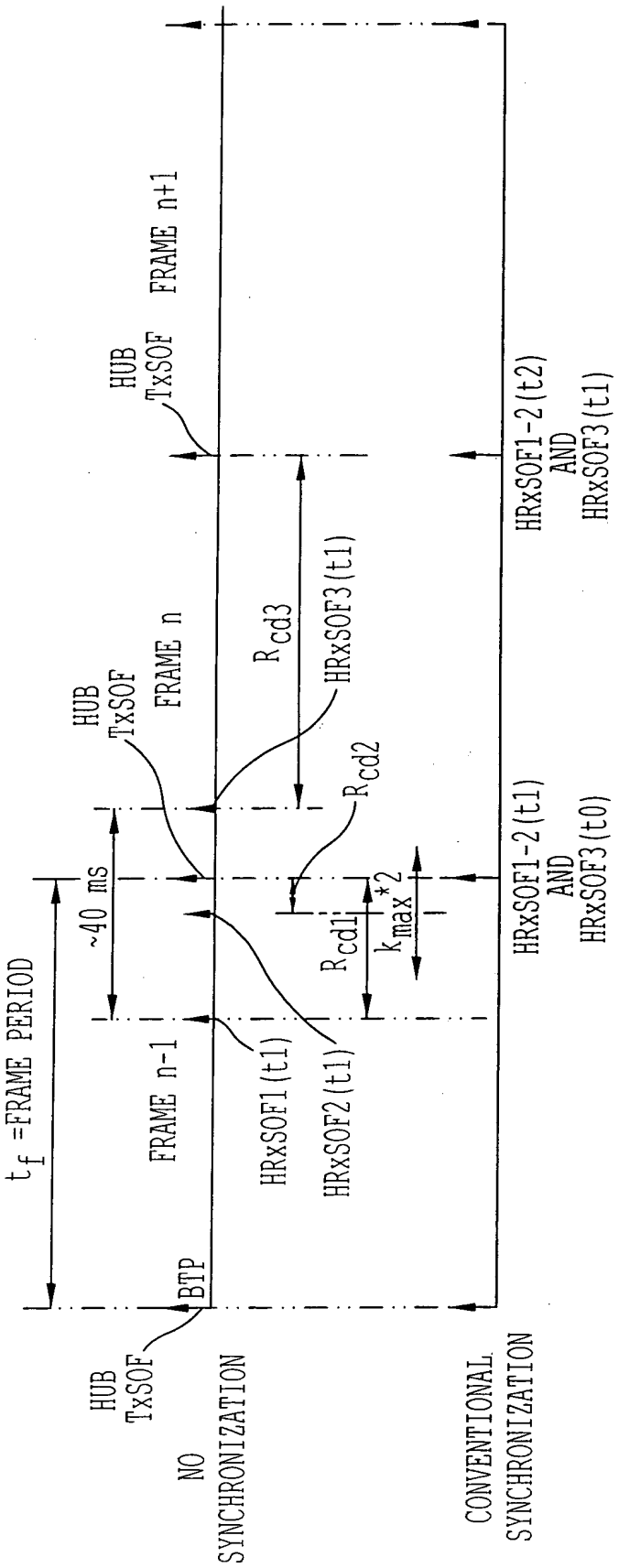


FIG. 3

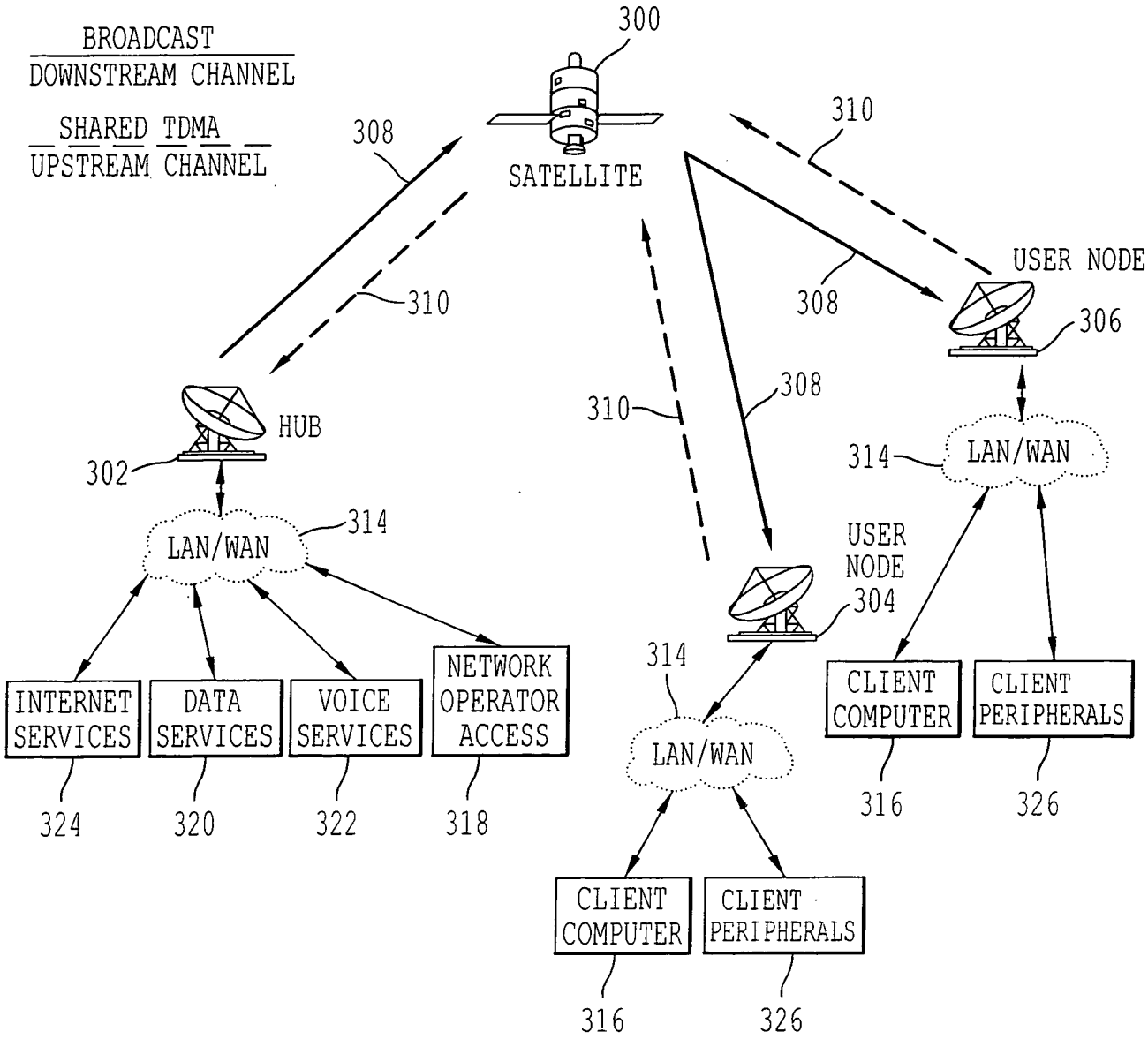
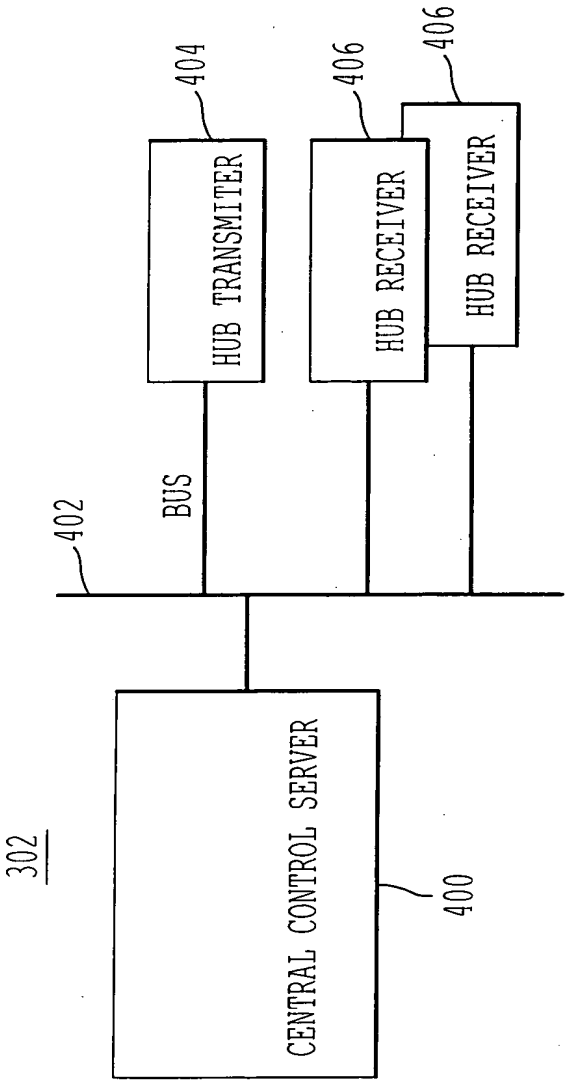

BROADCAST
DOWNSTREAM CHANNEL
SHARED TDMA
UPSTREAM CHANNEL
300
SATELLITE
308
310
310
308
USER NODE
306
HUB
302
310
308
314
LAN/WAN
314
LAN/WAN
USER
NODE
304
314
LAN/WAN
INTERNET
SERVICES
DATA
SERVICES
VOICE
SERVICES
NETWORK
OPERATOR
ACCESS
CLIENT
COMPUTER
CLIENT
PERIPHERALS
CLIENT
COMPUTER
CLIENT
PERIPHERALS
324
320
322
318
316
326
316
326

FIG. 4


302
CENTRAL CONTROL SERVER
400
402
BUS
HUB TRANSMITER
404
HUB RECEIVER
406
HUB RECEIVER
406

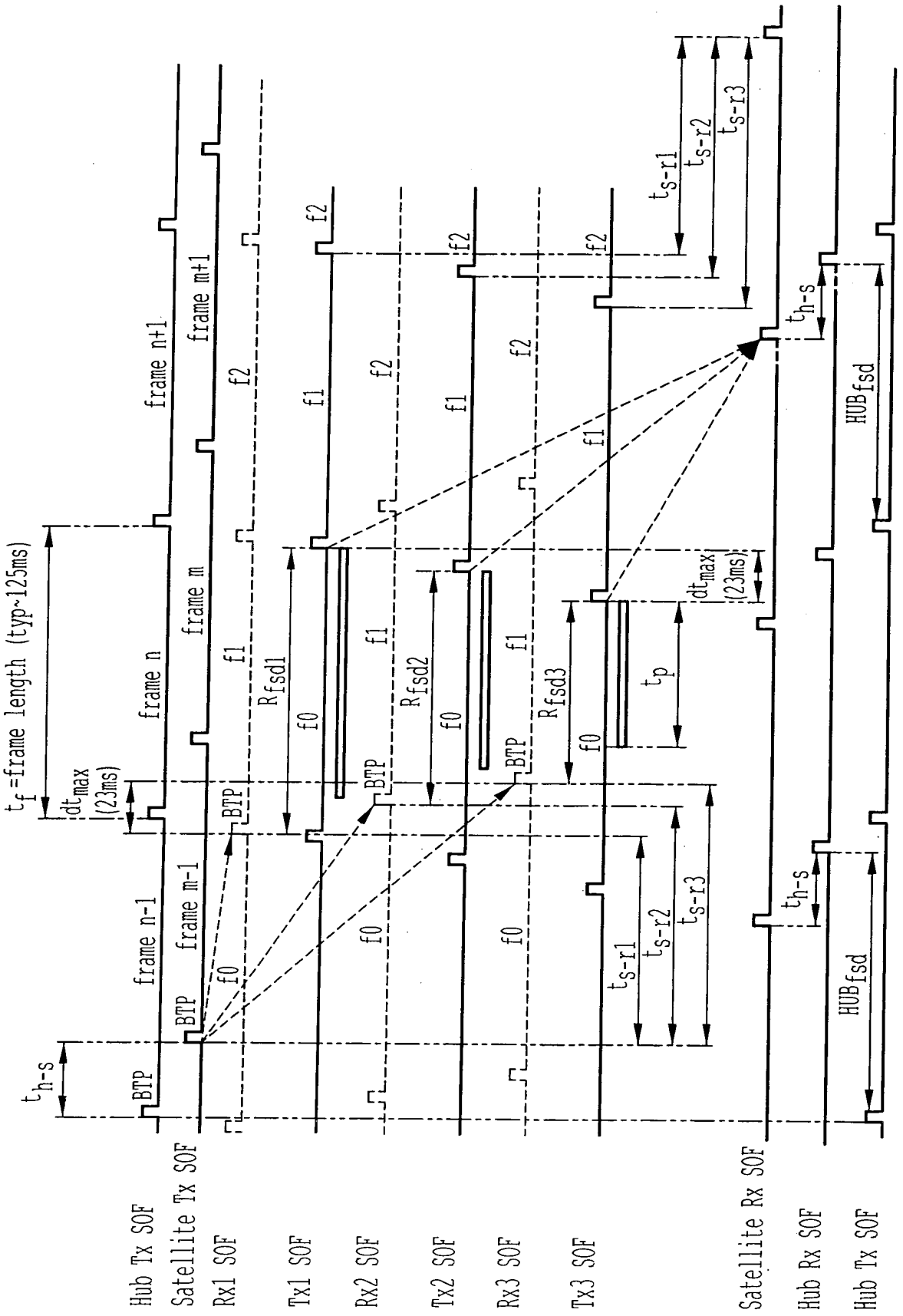

Hub Tx SOF
Satellite Tx SOF
Rx1 SOF
Tx1 SOF
Rx2 SOF
Tx2 SOF
Rx3 SOF
Tx3 SOF
Satellite Rx SOF
Hub Rx SOF
Hub Tx SOF
BTP
frame n-1
frame n
frame m-1
frame m
frame n+1
frame m+1
f0
f1
f2
t_f=frame length (typ~125ms)
dt_{max} (23ms)
t_{h-s}
R_{fsd1}
R_{fsd2}
R_{fsd3}
t_p
t_{s-r1}
t_{s-r2}
t_{s-r3}
HUBfsd

FIG. 5

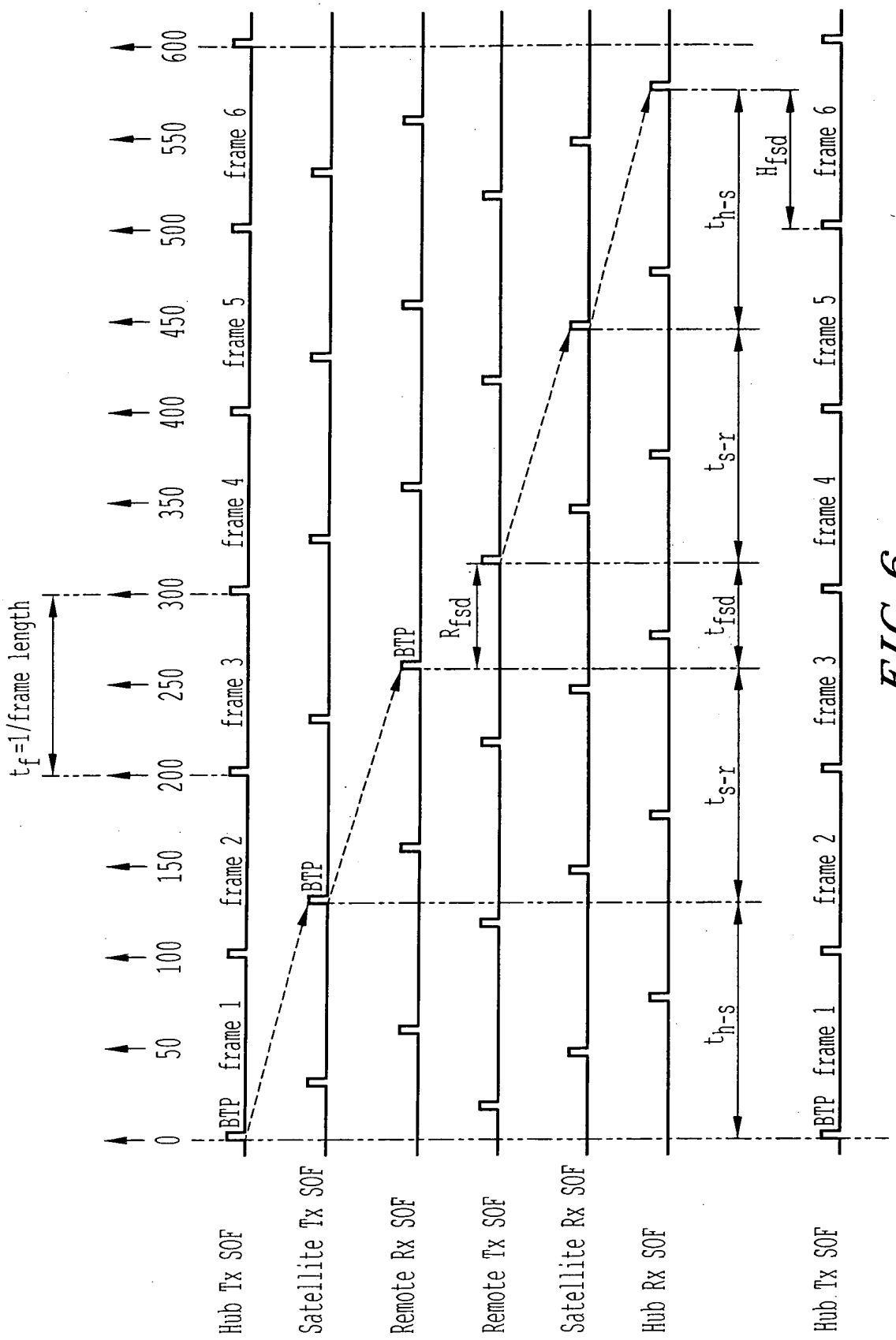

0
50
100
150
200
250
300
350
400
450
500
550
600
t_f=1/frame length
BTP
frame 1
frame 2
frame 3
frame 4
frame 5
frame 6
R_{fsd}
t_{s-r}
t_{fsd}
t_{h-s}
H_{fsd}
Hub Tx SOF
Satellite Tx SOF
Remote Rx SOF
Remote Tx SOF
Satellite Rx SOF
Hub Rx SOF
Hub Tx SOF

FIG. 6

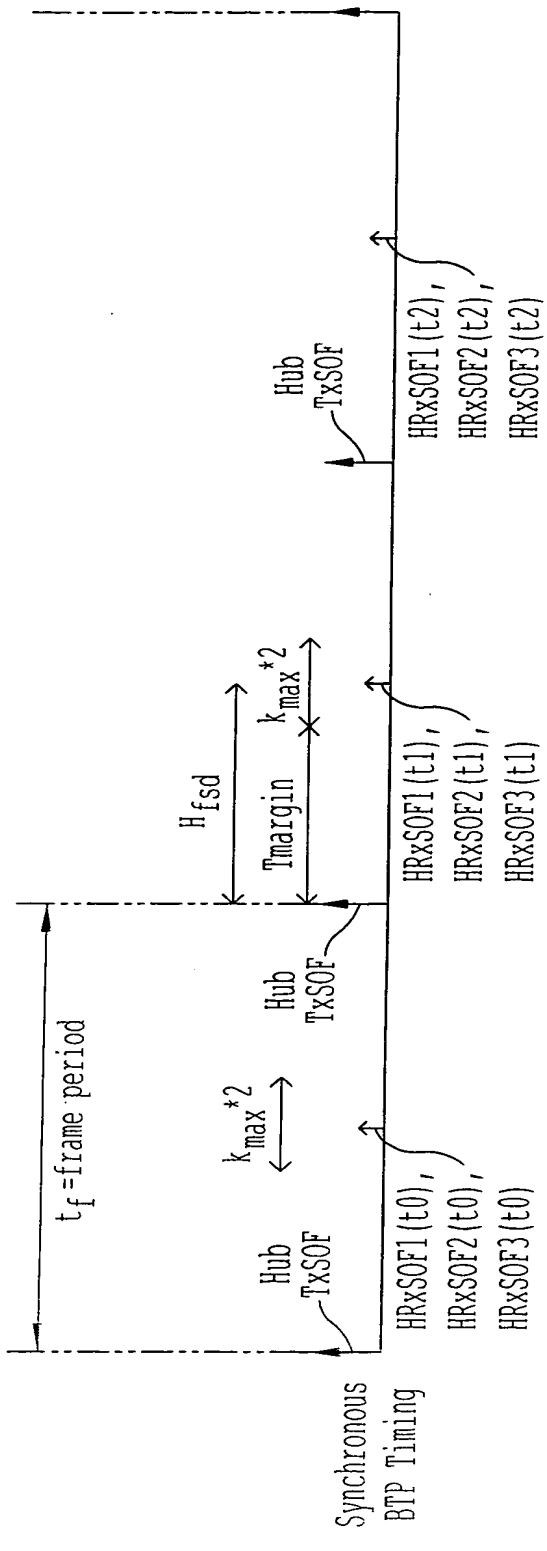

Synchronous BTP Timing
t_f=frame period
Hub TxSOF
k_{max}*2
Hub TxSOF
HRxSOF1(t0), HRxSOF2(t0), HRxSOF3(t0)
H_{fsd}
Tmargin
k_{max}*2
Hub TxSOF
HRxSOF1(t1), HRxSOF2(t1), HRxSOF3(t1)
HRxSOF1(t2), HRxSOF2(t2), HRxSOF3(t2)

FIG. 7

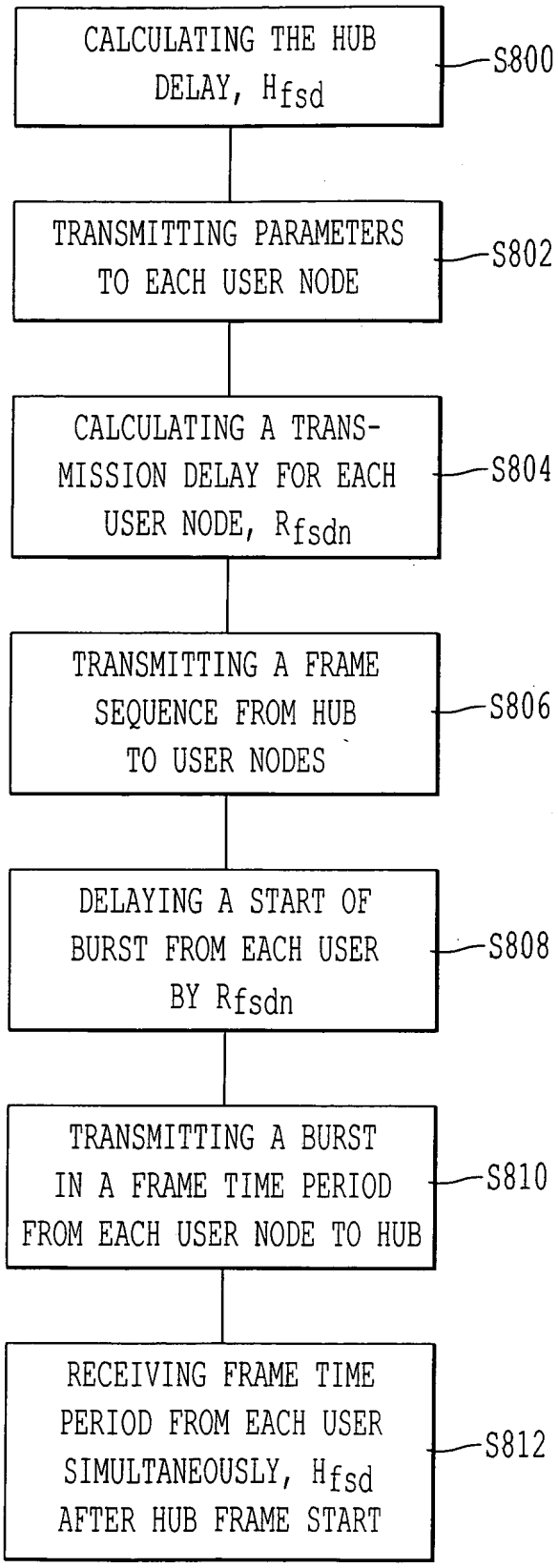

CALCULATING THE HUB DELAY, H_{fsd}
S800
TRANSMITTING PARAMETERS TO EACH USER NODE
S802
CALCULATING A TRANS-MISSION DELAY FOR EACH USER NODE, R_{fsdn}
S804
TRANSMITTING A FRAME SEQUENCE FROM HUB TO USER NODES
S806
DELAYING A START OF BURST FROM EACH USER BY R_{fsdn}
S808
TRANSMITTING A BURST IN A FRAME TIME PERIOD FROM EACH USER NODE TO HUB
S810
RECEIVING FRAME TIME PERIOD FROM EACH USER SIMULTANEOUSLY, H_{fsd} AFTER HUB FRAME START
S812

FIG. 8

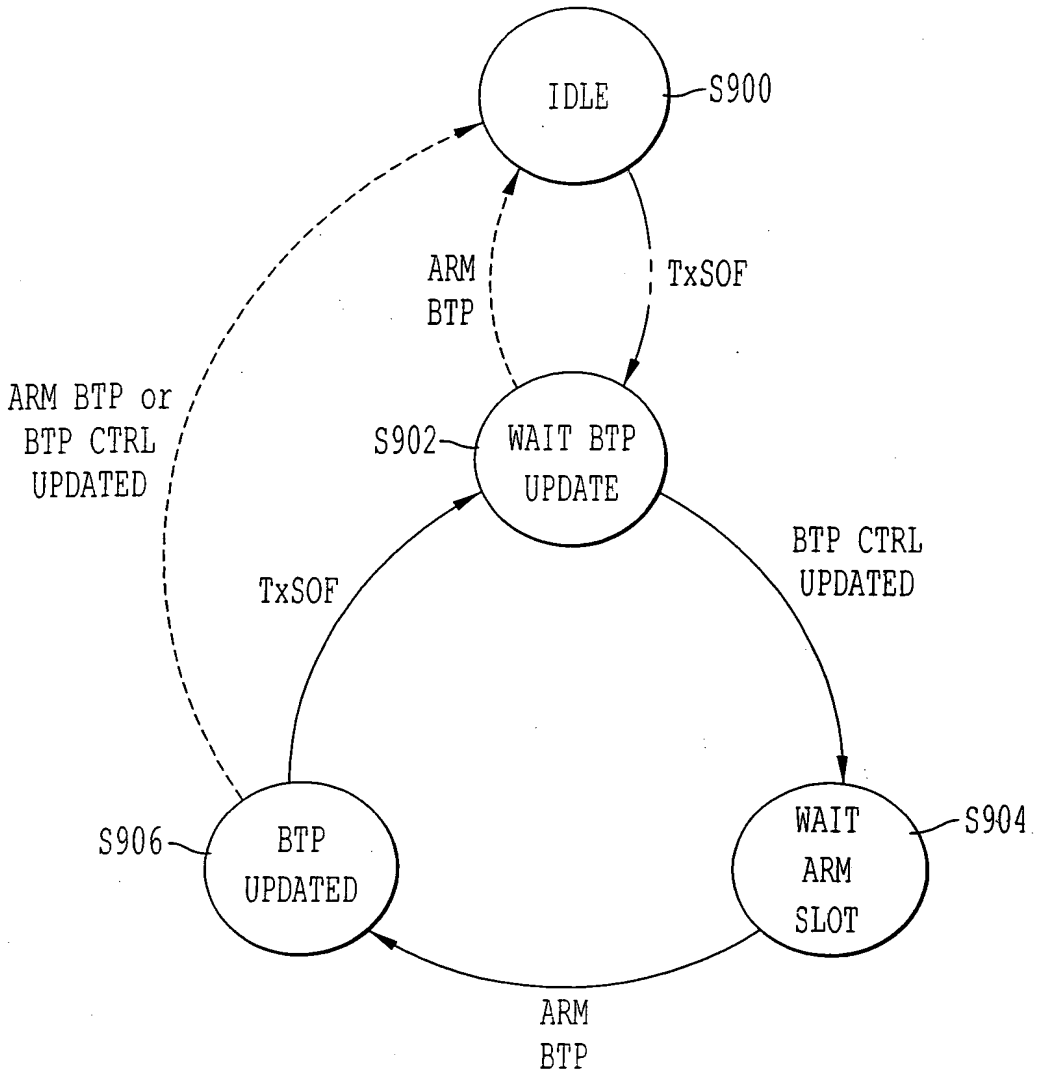

IDLE
S900
ARM
BTP
TxSOF
ARM BTP or
BTP CTRL
UPDATED
S902
WAIT BTP
UPDATE
BTP CTRL
UPDATED
TxSOF
S906
BTP
UPDATED
WAIT
ARM
SLOT
S904
ARM
BTP
NORMAL OPERATION
ERROR
ERROR RECOVERY

FIG. 9

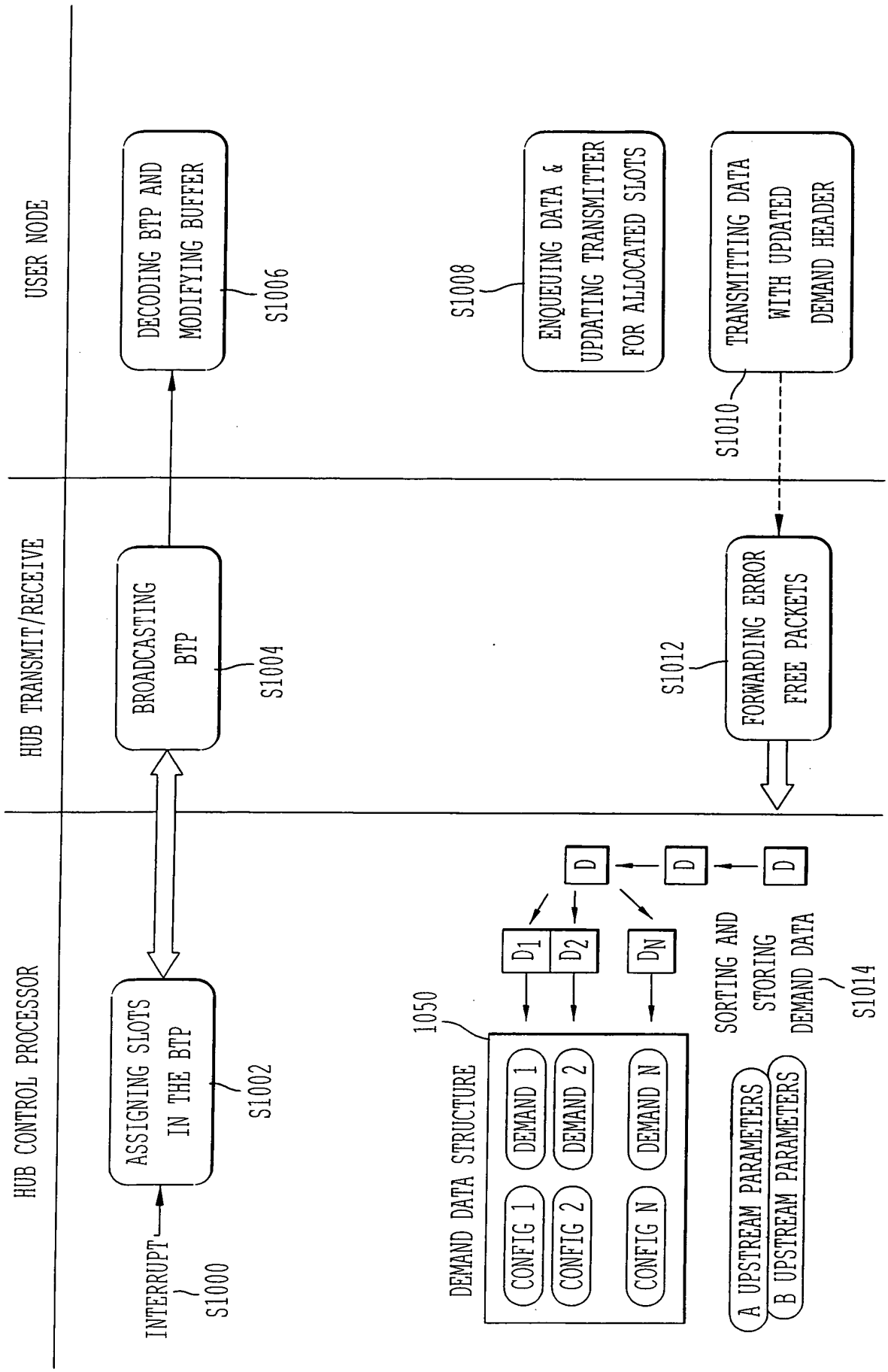

USER NODE
HUB TRANSMIT/RECEIVE
HUB CONTROL PROCESSOR
INTERRUPT
S1000
ASSIGNING SLOTS IN THE BTP
S1002
BROADCASTING BTP
S1004
DECODING BTP AND MODIFYING BUFFER
S1006
S1008
ENQUEUING DATA & UPDATING TRANSMITTER FOR ALLOCATED SLOTS
S1010
TRANSMITTING DATA WITH UPDATED DEMAND HEADER
S1012
FORWARDING ERROR FREE PACKETS
1050
DEMAND DATA STRUCTURE
CONFIG 1
CONFIG 2
CONFIG N
DEMAND 1
DEMAND 2
DEMAND N
D1
D2
DN
D
D
D
SORTING AND STORING DEMAND DATA
S1014
A UPSTREAM PARAMETERS
B UPSTREAM PARAMETERS

FIG. 10

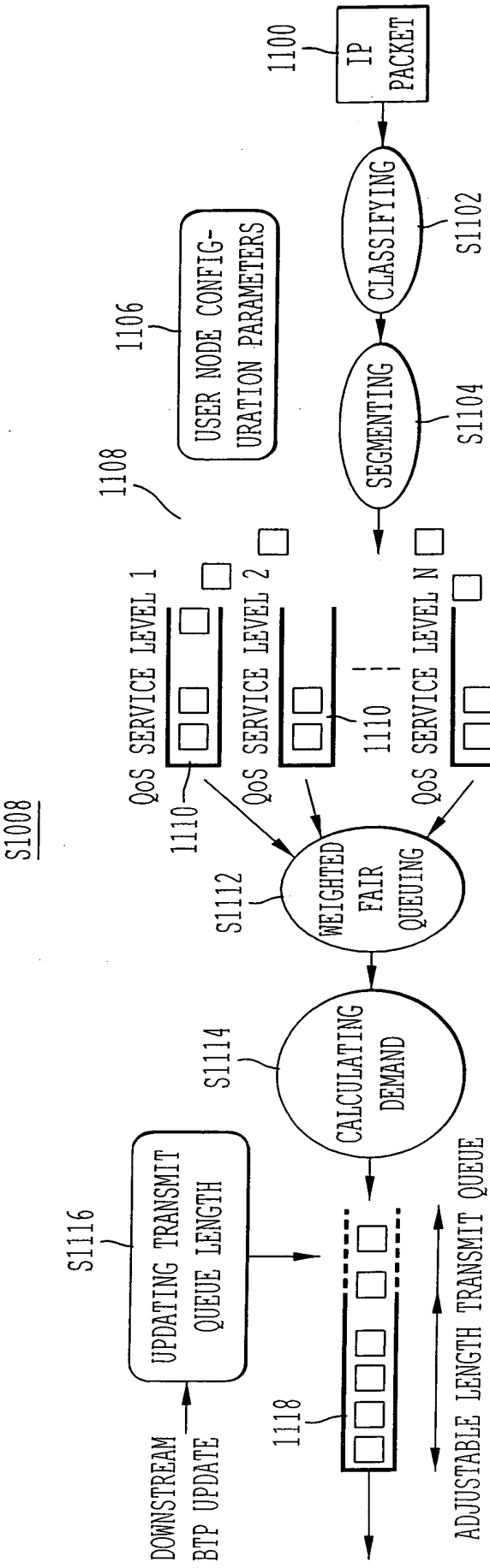

S1008
1100
IP PACKET
S1102
CLASSIFYING
S1104
SEGMENTING
1106
USER NODE CONFIG-URATION PARAMETERS
1108
QoS SERVICE LEVEL 1
QoS SERVICE LEVEL 2
QoS SERVICE LEVEL N
1110
1110
1110
S1112
WEIGHTED FAIR QUEUING
S1114
CALCULATING DEMAND
S1116
UPDATING TRANSMIT QUEUE LENGTH
DOWNSTREAM BTP UPDATE
1118
ADJUSTABLE LENGTH TRANSMIT QUEUE

FIG. 11A

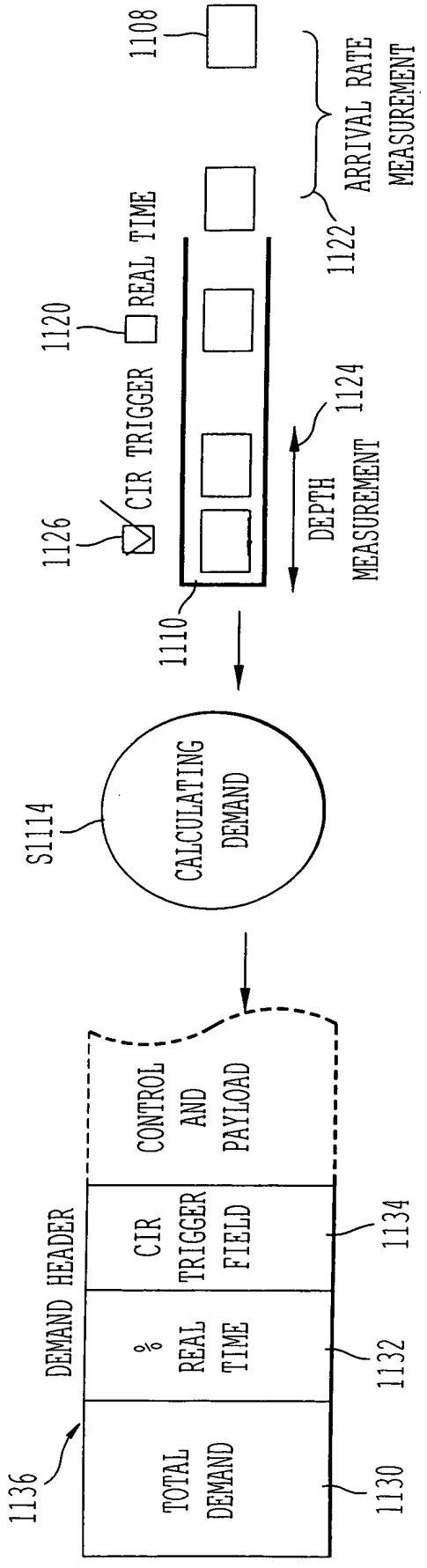

1108
ARRIVAL RATE MEASUREMENT
1122
1120
REAL TIME
CIR TRIGGER
1126
1124
DEPTH MEASUREMENT
1110
S1114
CALCULATING DEMAND
DEMAND HEADER
CONTROL AND PAYLOAD
CIR TRIGGER FIELD
1134
% REAL TIME
1132
TOTAL DEMAND
1130
1136

FIG. 11B

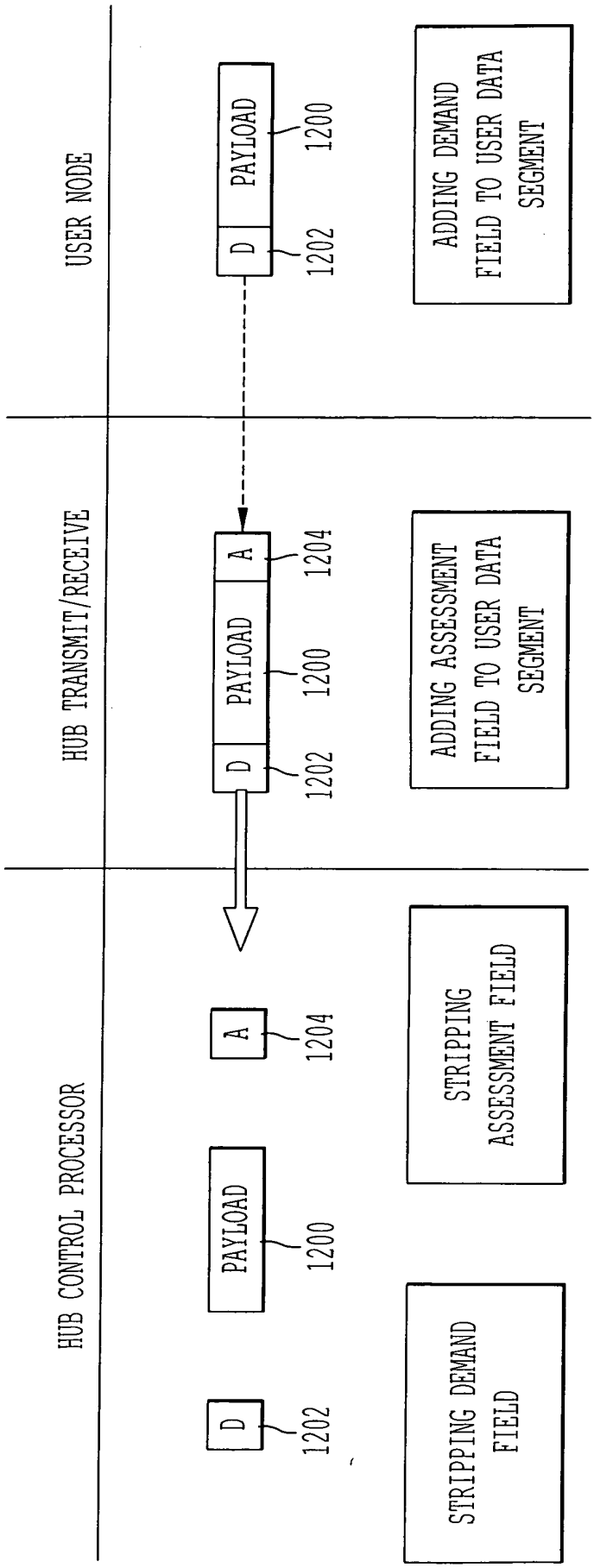

USER NODE
HUB TRANSMIT/RECEIVE
HUB CONTROL PROCESSOR
D
PAYLOAD
A
1202
1200
1204
ADDING DEMAND FIELD TO USER DATA SEGMENT
ADDING ASSESSMENT FIELD TO USER DATA SEGMENT
STRIPPING ASSESSMENT FIELD
STRIPPING DEMAND FIELD

FIG. 12

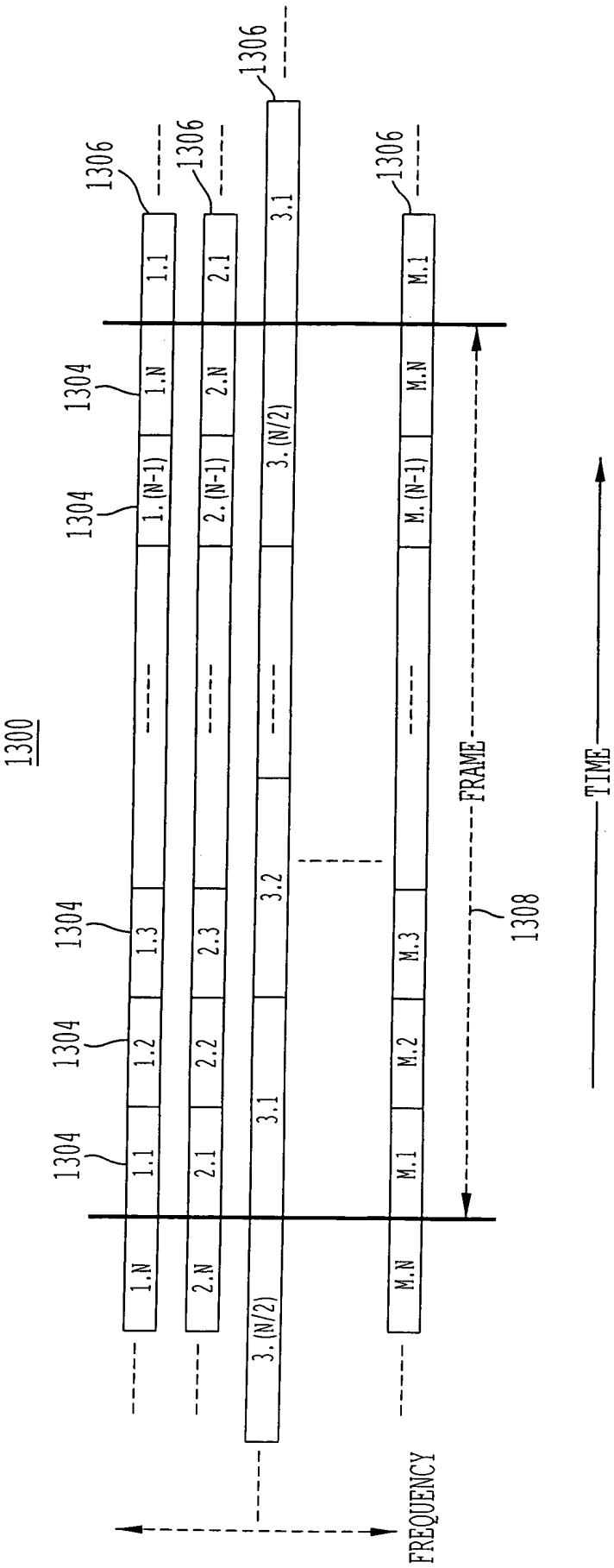

1300
1304
1306
1.1
1.2
1.3
1.N
1. (N-1)
2.1
2.2
2.3
2.N
2. (N-1)
3.1
3.2
3. (N/2)
M.1
M.2
M.3
M.N
M. (N-1)
FRAME
1308
TIME
FREQUENCY

FIG. 13

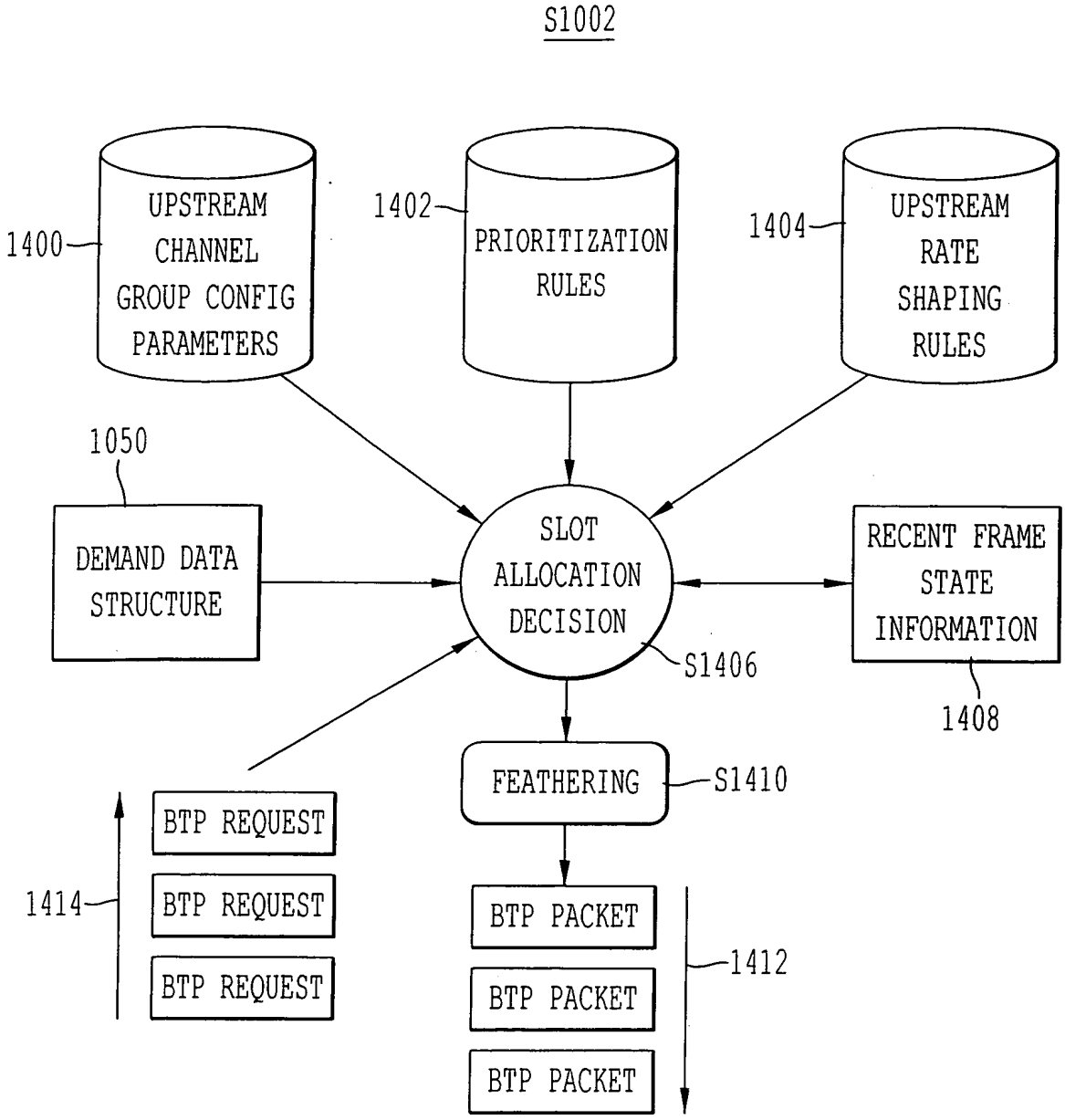
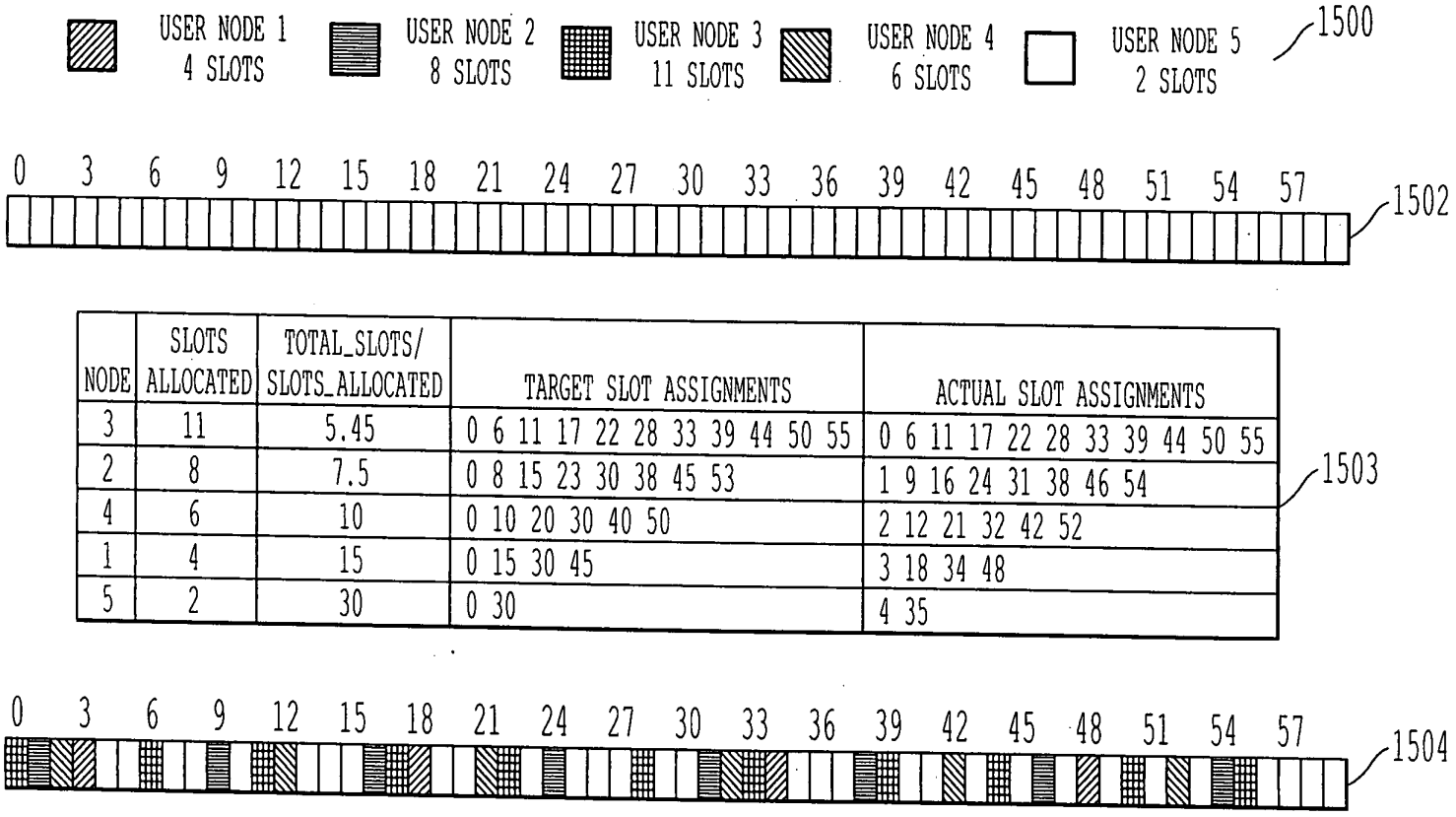

S1002
UPSTREAM CHANNEL GROUP CONFIG PARAMETERS
1400
PRIORITIZATION RULES
1402
UPSTREAM RATE SHAPING RULES
1404
1050
DEMAND DATA STRUCTURE
SLOT ALLOCATION DECISION
S1406
RECENT FRAME STATE INFORMATION
1408
FEATHERING
S1410
BTP REQUEST
BTP REQUEST
BTP REQUEST
1414
BTP PACKET
BTP PACKET
BTP PACKET
1412

FIG. 14



NODE	SLOTS ALLOCATED	TOTAL_SLOTS/ SLOTS_ALLOCATED	TARGET SLOT ASSIGNMENTS	ACTUAL SLOT ASSIGNMENTS
3	11	5.45	0 6 11 17 22 28 33 39 44 50 55	0 6 11 17 22 28 33 39 44 50 55
2	8	7.5	0 8 15 23 30 38 45 53	1 9 16 24 31 38 46 54
4	6	10	0 10 20 30 40 50	2 12 21 32 42 52
1	4	15	0 15 30 45	3 18 34 48
5	2	30	0 30	4 35

FIG. 15

OBLON, SPIVAK, et al
Docket No: 242845US8
Inventor: Conor FOLEY, et al.
Serial No: 10/721,419
Reply to NFMP dated: March 12, 2004
Replacement Sheet

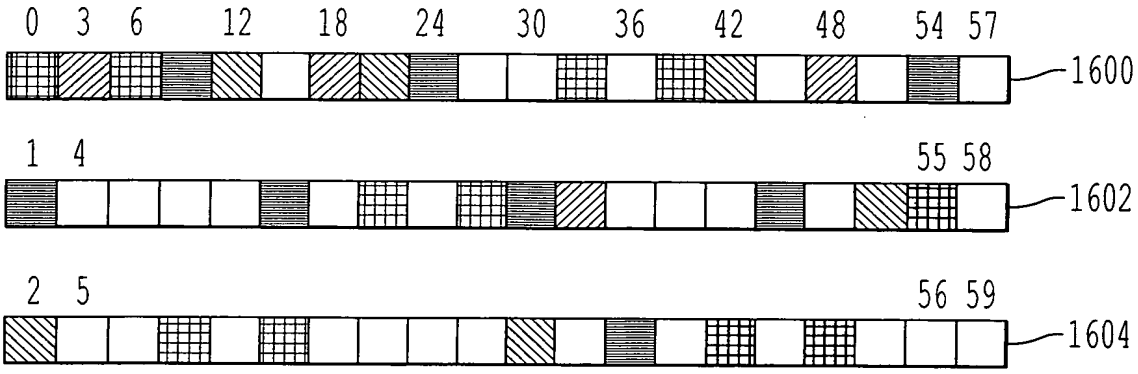

0 3 6 12 18 24 30 36 42 48 54 57
1600
1 4 55 58
1602
2 5 56 59
1604

FIG. 16

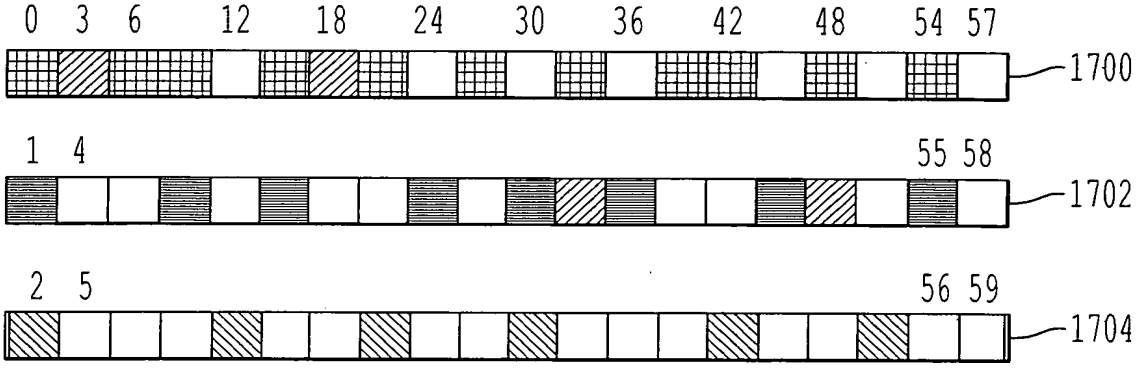

0 3 6 12 18 24 30 36 42 48 54 57
1700
1 4 55 58
1702
2 5 56 59
1704

FIG. 17

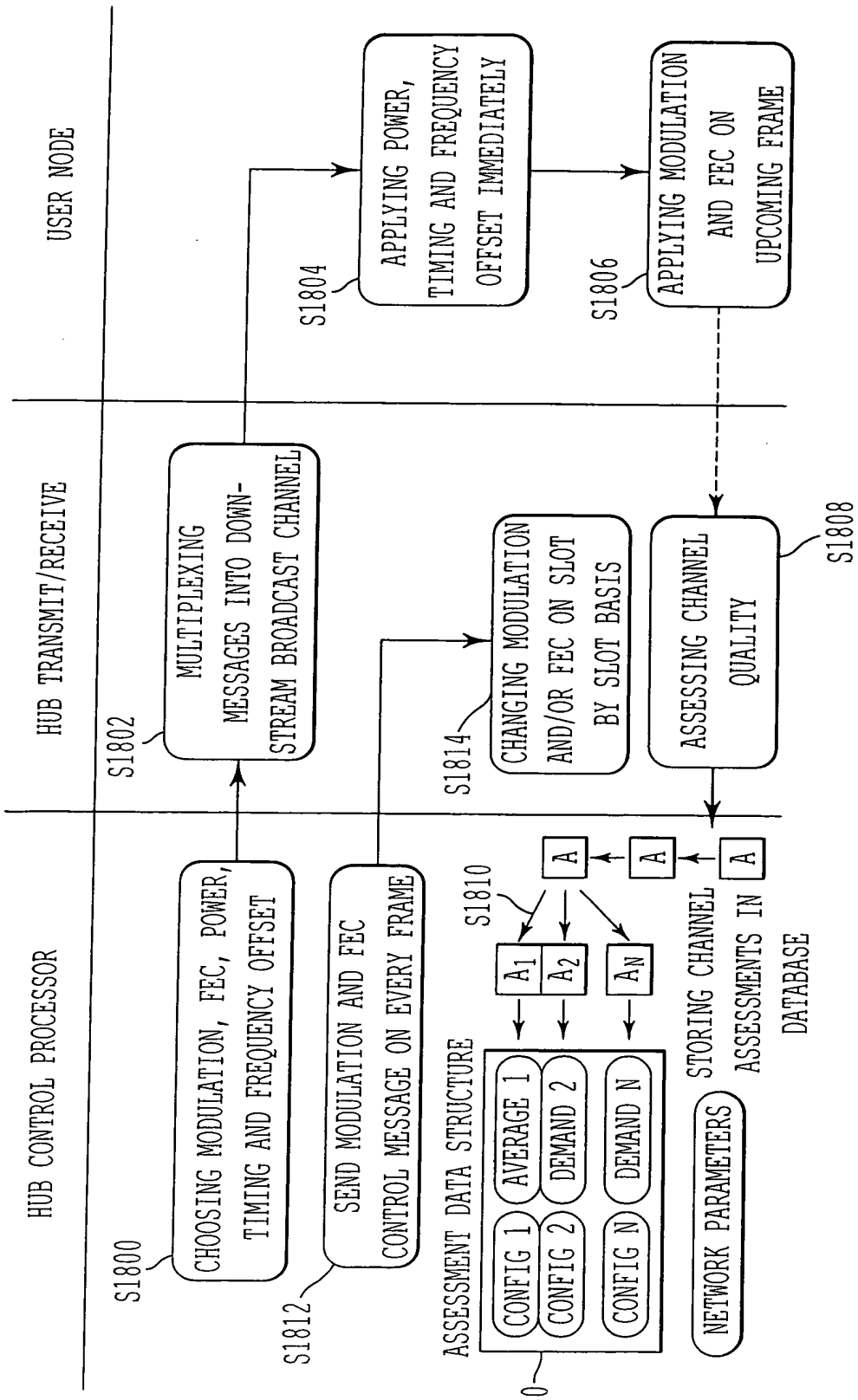

HUB CONTROL PROCESSOR
HUB TRANSMIT/RECEIVE
USER NODE
S1800
CHOOSING MODULATION, FEC, POWER, TIMING AND FREQUENCY OFFSET
S1802
MULTIPLEXING MESSAGES INTO DOWN-STREAM BROADCAST CHANNEL
S1804
APPLYING POWER, TIMING AND FREQUENCY OFFSET IMMEDIATELY
S1806
APPLYING MODULATION AND FEC ON UPCOMING FRAME
S1808
ASSESSING CHANNEL QUALITY
S1810
CHANGING MODULATION AND/OR FEC ON SLOT BY SLOT BASIS
S1812
SEND MODULATION AND FEC CONTROL MESSAGE ON EVERY FRAME
ASSESSMENT DATA STRUCTURE
CONFIG 1
CONFIG 2
CONFIG N
AVERAGE 1
DEMAND 2
DEMAND N
A1
A2
AN
A
A
A
STORING CHANNEL ASSESSMENTS IN DATABASE
NETWORK PARAMETERS
1850

FIG. 18

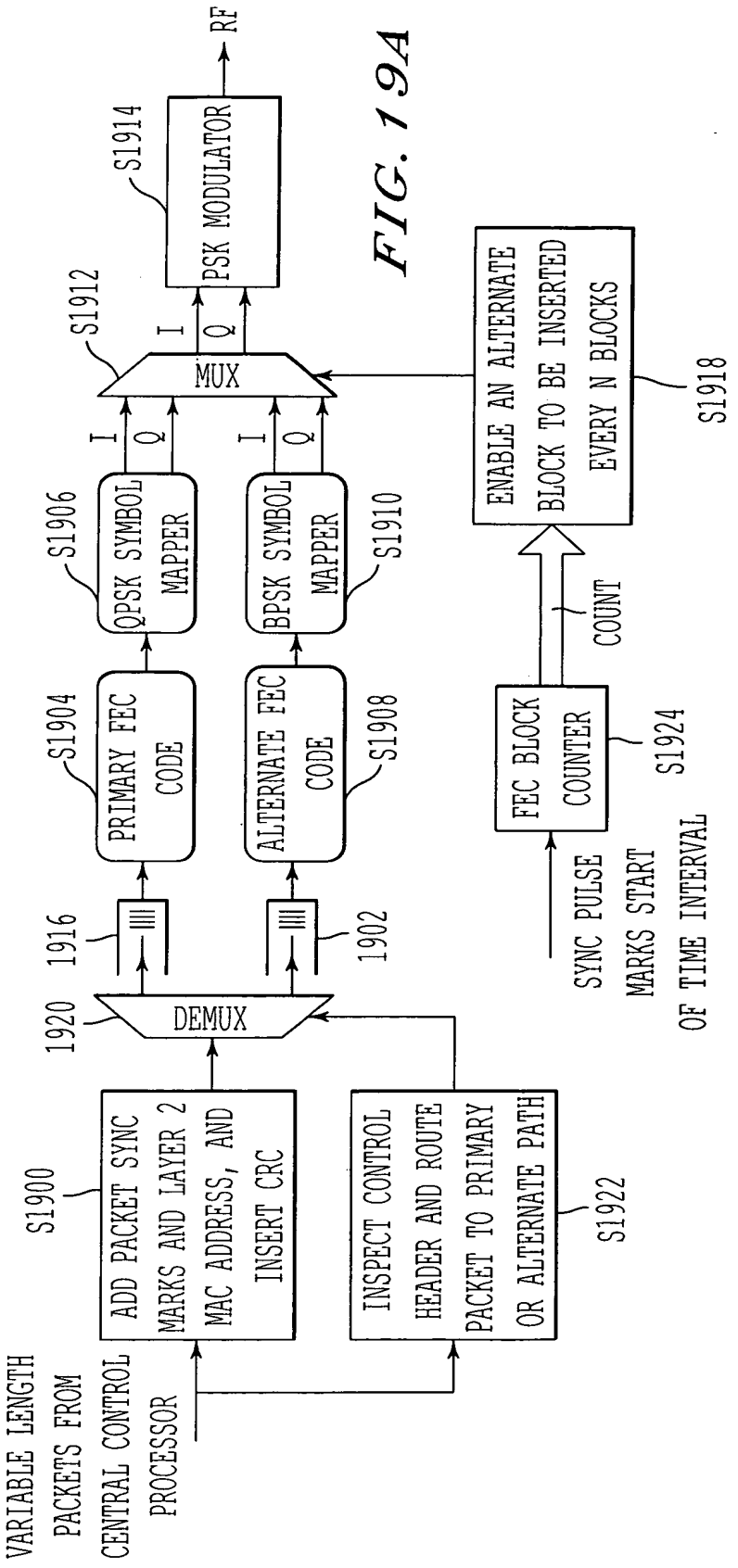
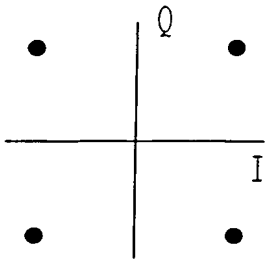
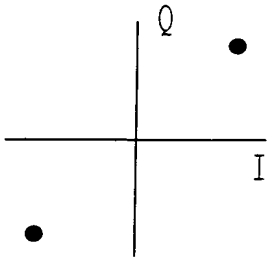

VARIABLE LENGTH PACKETS FROM CENTRAL CONTROL PROCESSOR
S1900
ADD PACKET SYNC MARKS AND LAYER 2 MAC ADDRESS, AND INSERT CRC
INSPECT CONTROL HEADER AND ROUTE PACKET TO PRIMARY OR ALTERNATE PATH
S1922
1920
DEMUX
1916
1902
S1904
PRIMARY FEC CODE
ALTERNATE FEC CODE
S1908
S1906
QPSK SYMBOL MAPPER
BPSK SYMBOL MAPPER
S1910
I
Q
S1912
MUX
S1914
PSK MODULATOR
RF
SYNC PULSE MARKS START OF TIME INTERVAL
FEC BLOCK COUNTER
S1924
COUNT
ENABLE AN ALTERNATE BLOCK TO BE INSERTED EVERY N BLOCKS
S1918

FIG. 19A



QPSK
CONSTELLATION

FIG. 19B



BPSK CONSTELLATION
ORIENTED AT 45 DEGREE
ANGLE TO BOTH AXES

FIG. 19C

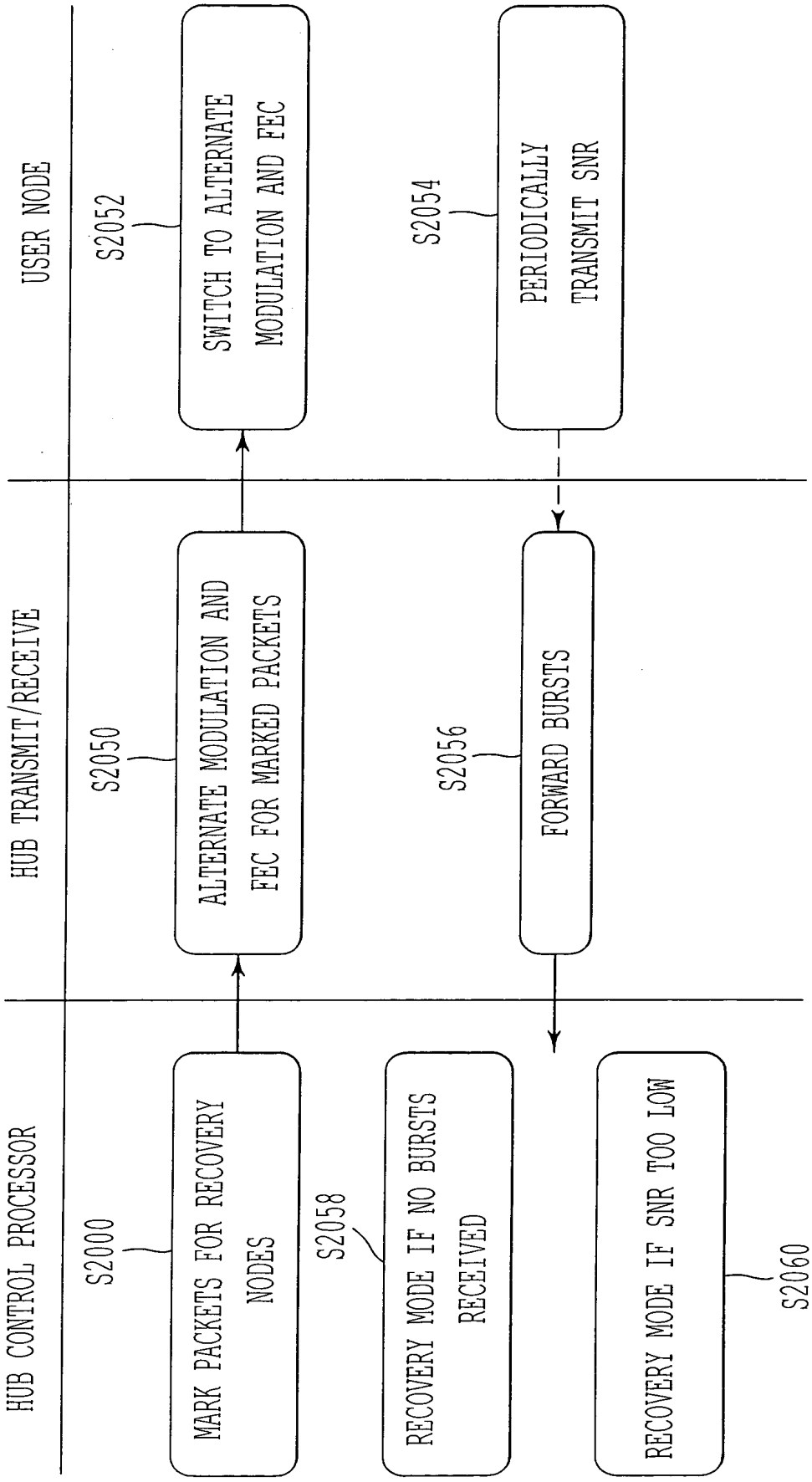

HUB CONTROL PROCESSOR
HUB TRANSMIT/RECEIVE
USER NODE
S2000
MARK PACKETS FOR RECOVERY NODES
S2050
ALTERNATE MODULATION AND FEC FOR MARKED PACKETS
S2052
SWITCH TO ALTERNATE MODULATION AND FEC
S2054
PERIODICALLY TRANSMIT SNR
S2056
FORWARD BURSTS
S2058
RECOVERY MODE IF NO BURSTS RECEIVED
S2060
RECOVERY MODE IF SNR TOO LOW

FIG. 20

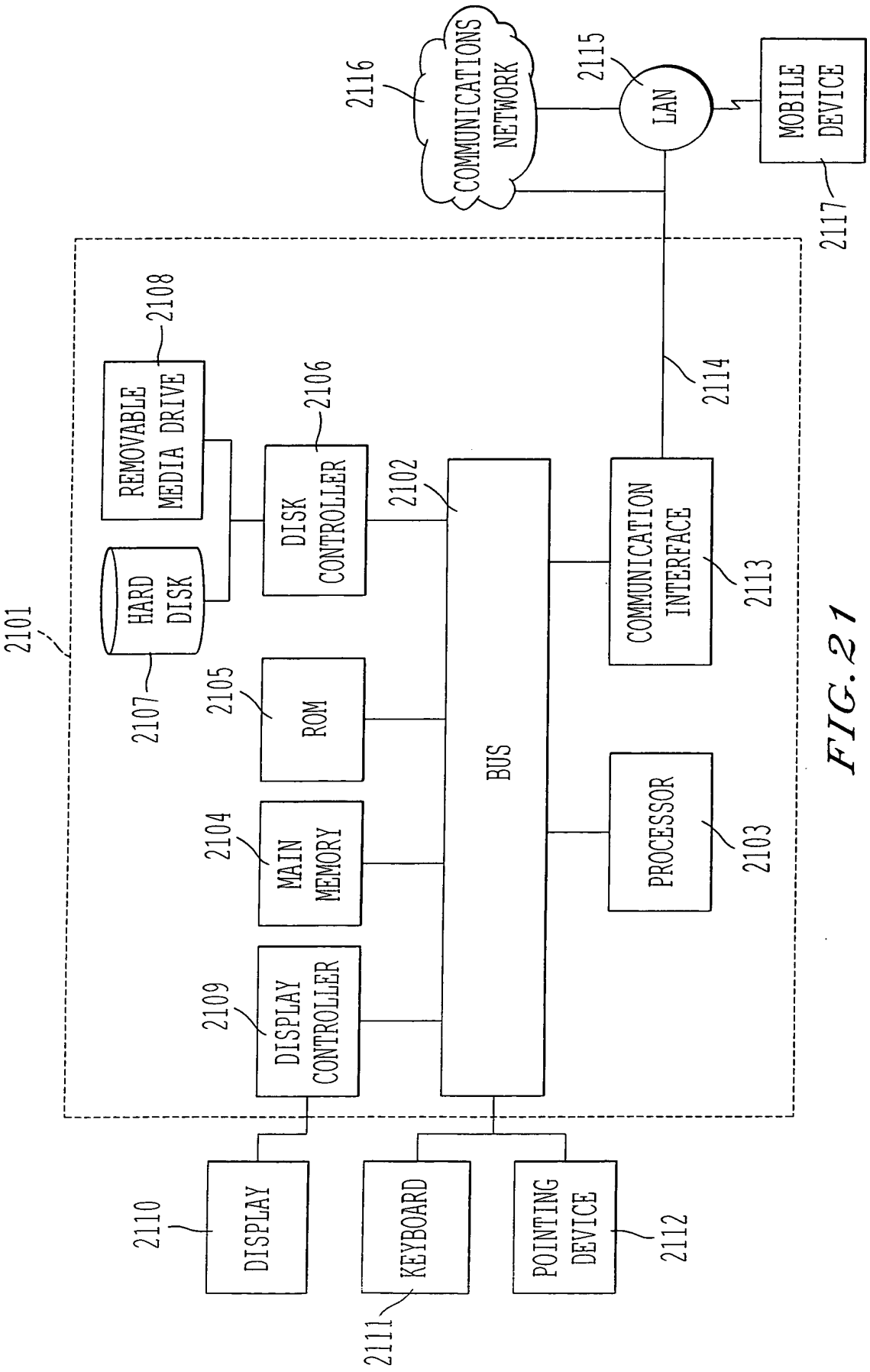

2116
COMMUNICATIONS NETWORK
2115
LAN
MOBILE DEVICE
2117
2101
2108
REMOVABLE MEDIA DRIVE
2106
DISK CONTROLLER
2102
2114
HARD DISK
2107
2105
ROM
BUS
COMMUNICATION INTERFACE
2113
2104
MAIN MEMORY
PROCESSOR
2103
2109
DISPLAY CONTROLLER
2110
DISPLAY
KEYBOARD
POINTING DEVICE
2112
2111

FIG. 21

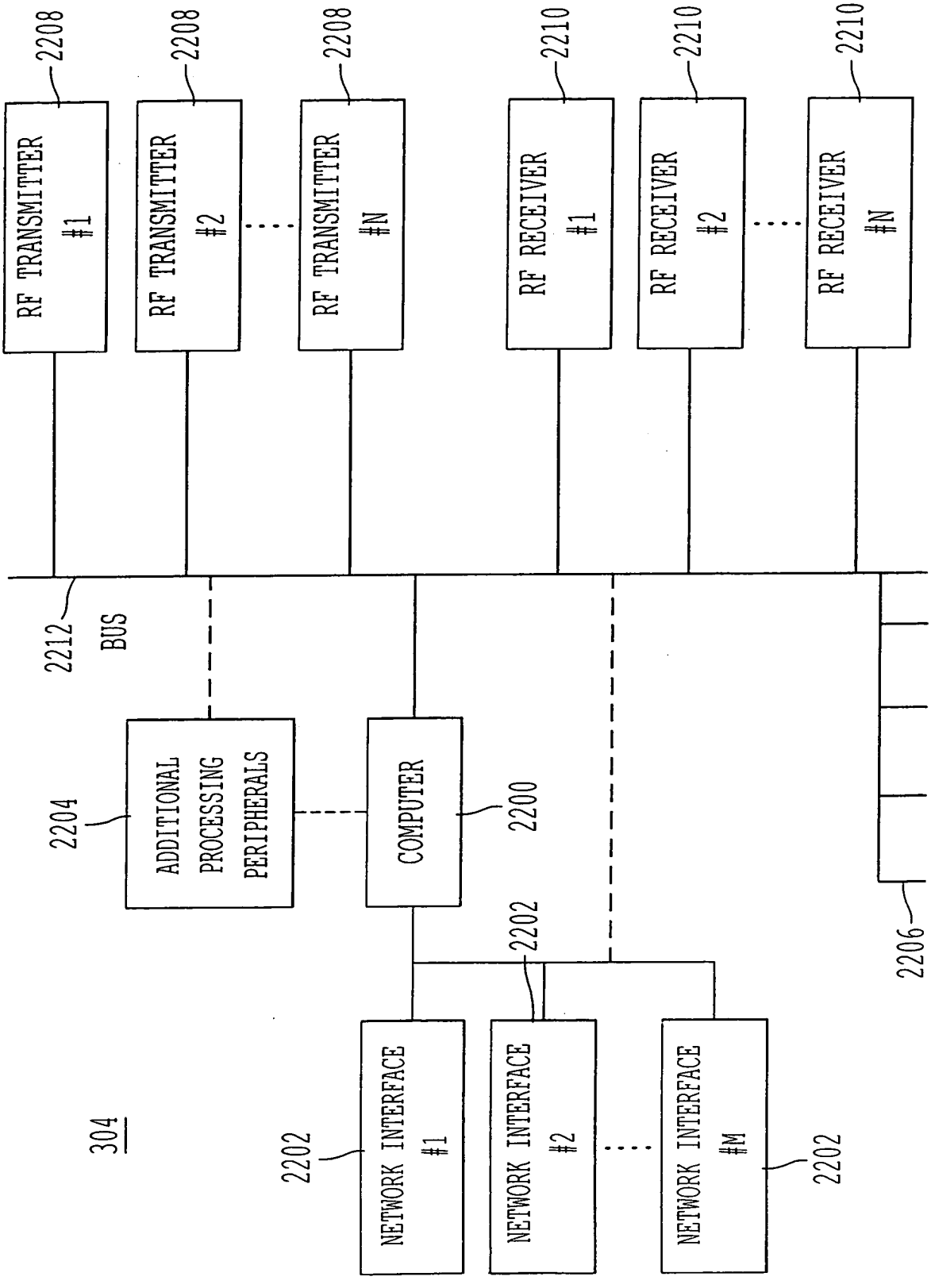

304
NETWORK INTERFACE #1
NETWORK INTERFACE #2
NETWORK INTERFACE #M
2202
2202
2202
ADDITIONAL PROCESSING PERIPHERALS
2204
COMPUTER
2200
BUS
2212
RF TRANSMITTER #1
RF TRANSMITTER #2
RF TRANSMITTER #N
2208
2208
2208
RF RECEIVER #1
RF RECEIVER #2
RF RECEIVER #N
2210
2210
2210
EXPANSION PERIPHERAL CONNECTIONS
2206

FIG. 22